L Number	Hits	Search Text	DB	Time stamp
1	21287	vco (voltage adj control$4 adj oscillator$1)	USPAT	2003/06/09 07:36
2	24401	agc (automati$4 adj gain adj control$4)	USPAT	2003/06/09 07:37
3	2238	(vco (voltage adj control$4 adj oscillator$1)) and (agc (automati$4 adj gain adj control$4))	USPAT	2003/06/09 07:41
5	41	spread adj spectrum adj clock	USPAT	2003/06/09 07:40
6	1	((vco (voltage adj control$4 adj oscillator$1)) near4 (agc (automati$4 adj gain adj control$4))) and (spread adj spectrum adj clock)	USPAT	2003/06/09 07:38
7	134	(spread adj spectrum) near3 clock	USPAT	2003/06/09 07:41
8	41	(spread adj spectrum adj clock) and ((spread adj spectrum) near3 clock)	USPAT	2003/06/09 07:41
9	1	((vco (voltage adj control$4 adj oscillator$1)) near4 (agc (automati$4 adj gain adj control$4))) and ((spread adj spectrum) near3 clock)	USPAT	2003/06/09 07:41
10	219	(spread adj spectrum) near5 clock	USPAT	2003/06/09 07:45
11	1	((vco (voltage adj control$4 adj oscillator$1)) near4 (agc (automati$4 adj gain adj control$4))) and ((spread adj spectrum) near5 clock)	USPAT	2003/06/09 07:41
12	547	(vco (voltage adj control$4 adj oscillator$1)) same (agc (automati$4 adj gain adj control$4))	USPAT	2003/06/09 07:41
13	4	((spread adj spectrum) near5 clock) and ((vco (voltage adj control$4 adj oscillator$1)) same (agc (automati$4 adj gain adj control$4)))	USPAT	2003/06/09 07:42
14	1987	spread same clock	USPAT	2003/06/09 07:46
16	2	((vco (voltage adj control$4 adj oscillator$1)) near4 (agc (automati$4 adj gain adj control$4))) and (spread same clock)	USPAT	2003/06/09 07:46
15	101	((vco (voltage adj control$4 adj oscillator$1)) and (agc (automati$4 adj gain adj control$4))) and (spread same clock)	USPAT	2003/06/09 08:27
17	22	(vco (voltage adj control$4 adj oscillator$1)) same ((spread adj spectrum) near3 clock)	USPAT	2003/06/09 08:27
4	63	(vco (voltage adj control$4 adj oscillator$1)) near4 (agc (automati$4 adj gain adj control$4))	USPAT	2003/06/09 08:49
18	254	nonlinear adj gain	USPAT	2003/06/09 08:50
19	18	(vco (voltage adj control$4 adj oscillator$1)) and (nonlinear adj gain)	USPAT	2003/06/09 08:59
20	18	(vco (voltage adj control$4 adj oscillator$1)) and (nonlinear adj gain)	USPAT	2003/06/09 08:59

US-PAT-NO: 5420543

DOCUMENT-IDENTIFIER: US 5420543 A
See image for Certificate of Correction

TITLE: Method and apparatus for determining a constant gain of
a variable oscillator

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Brief Summary Text - BSTX (11):
As microprocessor frequencies increase, it becomes necessary to deskew internal and external clocks. It is also desirable to run internal clocks faster than system clock rates. An analog phase-locked loop (PLL) has previously performed this function; however, as low-power applications for microprocessors proliferate, techniques for the implementation of on-chip power management are required. Generally, the implementation of a phase-locked loop (PLL) requires the acquisition of an appropriate frequency and phase using an internal ring oscillator. Analog phase-locked loops typically use a voltage-controlled oscillator (VCO) to generate a period signal that is "locked" to a reference clock signal.

Brief Summary Text - BSTX (12):
The frequency of the VCO is modulated by an analog voltage adjusted via a feedback mechanism. Typically, the feedback mechanism is supplied from a sequential phase/frequency detector. The sequential phase/frequency detector outputs an "up" or "down" pulse proportional to phase error width and in the direction required to pull in the frequency of the VCO

output signal to the target reference clock signal. The output of a sequential phase/frequency detector usually enables a charge pump driving to a loop filter (RC), which in turn controls the frequency of the VCO. The detector outputs can be arbitrarily small, and thus there is usually a dead band associated with such a detector where, for a certain window of time, there is no detectable output. Accordingly, during the dead band ("window width"), the PLL can detect neither "up" nor "down" pulses for a phase/frequency error of a magnitude equal to or less than the window width. This technique has been used in many applications, and requires careful tuning to maintain the right damping characteristics.

Brief Summary Text - BSTX (13):

In the PLL, the gain of the VCO is defined as dF/dV (the change in VCO frequency per change in the analog control voltage). Ideally, a linear gain is preferred, but a linear gain can only be approximated. Instead, there is a nonlinear gain, resulting in a gain curve. Several parameters can impact the gain (e.g. VDD, temperature, processing, etc.). These parameters cause shifts in the gain curve and also impact the slope of the gain curve. Thus, over different operating conditions, there is a family of gain curves, each corresponding to different sets of conditions. A given increment in an analog control voltage can, therefore, cause substantially different changes in the VCO frequency depending upon the operating conditions. This phenomenon adversely affects the stability and limits the range and performance of the PLL. For example, the gain may be very high for a given set of conditions, resulting in excessive PLL output jitter. Alternatively, the gain may be low,

resulting in an inability of the PLL to track frequency drift. It is, therefore, desirable to have a PLL wherein the gain tracks the operating point across all gain curves.